ABSTRACT

A new method of fabricating self-aligned, anti-via interconnects has been achieved. A semiconductor substrate is provided. A metal layer is deposited overlying the semiconductor substrate. The metal layer may comprise a composite stack of two metal layers. The metal layers may additionally be separated by an etch stopping layer. An anti-reflective coating layer is deposited overlying the metal layer. The metal layer is etched through to form connective lines. The metal layer is then etched partially through to form vias. The partial etching through may be accomplished by timed etching or by use of the optional etching stop layer. A dielectric layer is deposited overlying the vias, the connective lines and the semiconductor substrate. The dielectric layer may comprise a low-k material. The dielectric layer is polished down to complete the self-aligned, anti-via interconnects in the manufacture of the integrated circuit device.